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Implementation of Low Power SAR ADC Architecture Using Dual Tail Comparator

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Abstract

The comparator is one of the fundamental building block in ADC applications This paper presents based on comparator analysis in the ADC design to optimize power and area, maximize speed and clock frequency. According to an analytical expressions, designers can obtain an intuition about the main contributors to the comparator delay and fully explore the tradeoffs in dynamic comparator is proposed in the circuit of a dual tail comparator. Dual tail comparator is modified for low power and fast operations even in small supply voltages by adding few transistors, positive feedback during the regeneration is strengthened, it results to reduce delay time in the layout simulation results by using CMOS technology analysis. Power consuming for comparator is 0.252 mW and reducing 50% of area of the architecture due transistor sizing using 180 nm method and also improving latch regeneration speed.

Keywords:-Dual tail comparator, successive approximation, successive approximation register (SAR) ADC, sampling capacitor's, reference DAC, Input capacitance and switches.

Introduction

The comparator block is the major key element for design ADC architectures. It help us to optimized equality of the comparators for general purpose processor components and the logic design is straight forward ,an extensive use of comparators in the high performance systems places a great importance in the performance and power consumption optimizations. The artwork of the comparator design uses dynamic gate logic circuit structures to enhance performance while other leverage specialized arithmetic units for wide comparisons along with custom logic circuits.

Many high speed ADC's such as flash ADC's require high speed, low power comparators with small chip area. High speed comparators in Ultra Deep Sub Micrometer (UDSM) CMOS technologies suffer from low supply voltages especially by considering threshold voltages of the devices cannot be scaled at the modern CMOS processes. Hence designing high speed comparators is more challenging with the supply voltage is smaller. To achieve high speed, large transistors are required to compensate the reduction of supply voltage. Besides low voltage operation results in limited common mode inputs range, it's an important factor for many high speed ADC architecture and the techniques such as supply boosting method, body driven transistors, current mode design and those using dual oxide processes and it deals with higher supply voltages have been developed to meet the low voltage design challenges.

The supply boosting technique is based on supply, reference or clock voltage to address an input range and switching problems its an effective method, but they introduce reliability issues such as in UDSM CMOS technology. Body driven technique is adopted by blalock to remove threshold voltage requirement such as body driven MOSFET operates as a depletion type device based on this approach by introducing a single bit quantizer modulators in proposed method. The body driven transistor suffers from smaller transconductance compared with gate driven counter, while special fabrication process such as deep n-well is required and it operate in the body driven configuration. A part from these technological, developing new circuit structures it avoids stacking too many transistors between the supply rails is preferable for low voltage operation especially for reducing the circuit complexity. In additional circuitry is added to the conventional dynamic comparator to enhance comparator speed in low supply voltages.

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The proposed comparator works to optimize the supply voltage with a maximum clock frequency. The effectiveness of this approach the effect of component mismatch in the additional circuitry performance of comparator should be considered the structure of dual tail comparator is proposed based on designing separate input and cross coupled stages. The separate input and cross coupled stage helps to enables fast operation over a wide common mode and supply voltage range. The dual tail comparator structure does not required boosted voltage of too many transistors it required a few minimum size transistors, it required a few minimum size transistors are used to reduced delay time and power savings when compared with dynamic comparator. The comparator and sampling switches are the only analog components of the SAR ADCs, and no other blocks consumes static power. For higher conversion rate applications the SAR ADCs are power and area efficient architecture by using CMOS technology. In conversion process common mode voltage variations of the comparator vary from Vcm and Vrefn it affects the ADC linearity. The DAC switching energy does not consume switching energy at initial stage so it can effectively reduce power consumption and design effort of the reference buffer.

Overview Of Design Concept Of The Proposed Method

A.ADC Architecture

The proposed block diagram of ADC. It consists of sampling capacitors, capacitive reference DACs, dynamic latched comparator and SAR control logic. The capacitive DAC is split into two parts a reference DAC and a sampling capacitor. The sampling capacitor captures the input signal and the reference DAC provides the reference signal. The reference DAC is a binary weighted capacitor array which has better linearity than the capacitor array with a bridged capacitor.

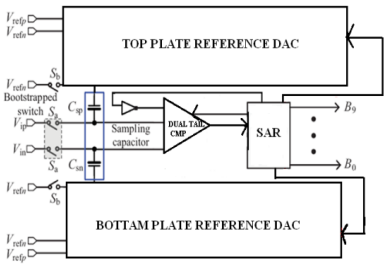

Fig 2.Block diagram of the present SAR ADC

In the sampling phase functioning consist of two steps based on it

Step 1:-The initial stage is switches S_a and S_b are in ON condition the input signals is sampled onto the sampling capacitors, C_{sp} and C_{sn}. The most significant bit of the bottom plate capacitor in the references DAC is switched to V_{refp} and those of the least significant bits are switched to V_{refn} at a time, but reference digital to analog comparator is in the reset stage.

Step2:-If the switches Sa and Sb are in off condition, then SAR ADC act be 0.The MSB triggers the SAR logic to control the reference switching than Vin then MSB set to be as 1.If Vip is less than Vin then MSB set to be in DAC by the switchback switching step.

B.SWITCHBACK SWITCHING PROCEDURE

The switchback switching procedure of the monotonic switching procedure only switches a capacitor in every bit cycles, so it reduces the charge in the capacitive DAC network as well as the transitions of the control circuit and switch buffer, it results the low power dissipation. The switchback switching procedure of the common mode variation would be below in initial state of the switching and above for the remainder. The large variation of the common mode voltage is quarter of the Vref and common mode voltage will be gradually approach the input signal of common mode voltage is Vcm. It decreases the dynamic offset and parasitic capacitance variations in the comparator.

Where a 10 bit binary weighted capacitive DAC is adopted and it is the same as the reference DAC adopted from figure 2 removed by figure 3 by illustrating as a sampling capacitor in switchback switching procedure .The quantitative energy consumption of the initial tri switching phase is shown in the above figure 3.The bottom plate capacitor of the MSB is connected to the Vrefp and the remaining are connected to the Vrefn at the sampling phase in the switchback switching method .In the sampling phase switches are turn off condition ,so the comparator is directly functioning the initial comparison without switching any capacitor .After that single MSB capacitor will switch to Vrefn ,there is no energy consumption in the conversion process.The below figure 3 shows the model of the switchback switching method.

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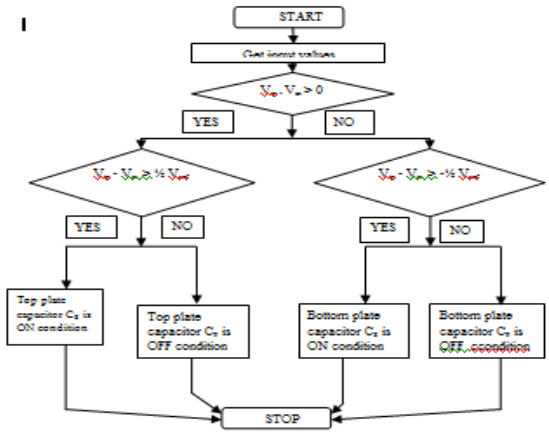

Fig 3. Switchback switching procedure of 10 bit SAR ADC

In the n-bit SAR ADC every digital output code is equiprobable an average switching energy of monotonic switching derived as

$$E_{avg,mono} = \sum_{i=1}^{n-1} (2^{n-2-i}) CV_{ref}^2$$

For the switchback switching procedure the average switching energy of n-bit SAR ADC is derived as

$$E_{avg,switch} = \sum_{i=1}^{n-2} (2^{n-3-i}) CV_{ref}^2$$

The reference voltage, Vref is calculated as given below

$V_{ref} = V_{ref} - V_{refn}$

Where,

C is the unit capacitance of the DAC.

V_{ref} is the reference voltage supply to reference DAC.

For a 10-bit SAR ADC in switchback switching procedure the average switching energy of monotonic switching method is 255.5 CV^2_{ref}.The a 10-bit SAR ADC in switchback switching procedure the average switching energy of V_{cm} based switching method is 170.2 CV^2_{ref}.And the proposed switching method consumes 127.5 CV^2_{ref}.Thus the proposed method requires 50% lesser switching energy compare with the previous two methods. The graphical representation of switching energy versus output code comparison is given below in figure 4.

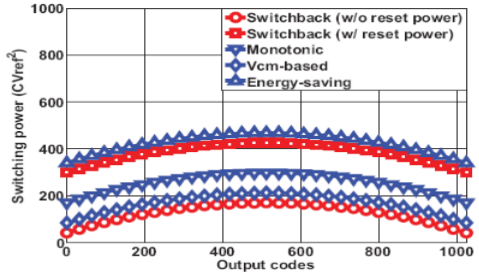

Fig. 4. Switching energy versus output code

The switchback switching method consumes low power compare with the monotonic and Vcm based switching methods during the conversion phase. In the sampling phase it must be pre-charging .For a 10-bit case all of the switching methods sample the same input signal, switchback switching method uses 255.5 CV^2_{ref}.Fig 4 shows a comparison of switching energy with four methods and its output code in both sampling phase and conversion phase are measured.

According to the switchback switching method does not consume more power than the Vcm based and monotonic switching methods in the conversion phase and sampling phase are taken in to considered .Note that switchback switching energy method reduces the design effort of the reference voltage of the circuit .The most significant bit capacitor must settle to the reference voltage in very less time during in the conversion phase .In the sampling phase the MSB capacitor of switchback switching method in pre-charge phase. Therefore it does not required a fast settling reference buffer to charge most significant capacitor in the conversion phase.

C .SAR CONTROL LOGIC

Successive approximation register ADCs are more compatible with technology scaling because they do not need operational amplifiers and have fewer floating switches. The only analog part is the comparator, whose design is similar to that of the digital regenerative latch. To compare with the pipeline architecture and SAR architecture would still be a better choice for low power and act as ADCs.

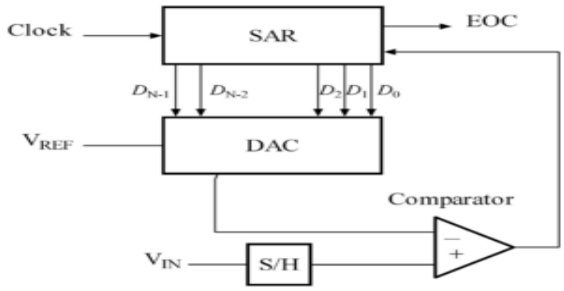

Fig 5 General block diagram for SAR

Where,

- DAC = Digital-to-Analog converter
- EOC = End Of Conversion
- SAR = Successive Approximation Register
- S/H = Sample and Hold Circuit
- V_{in} = Input Voltage
- V_{ref} = Reference Voltage

The Successive approximation register (SAR) analog-to digital converters (ADCs) require several comparison cycles to complete one conversion, and therefore have limited operational

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speed. SAR architectures are extensively used in low-power and low-speed (below several MS/s) applications. Successive approximation register (SAR) do not need operational amplifiers and have fewer floating switches. The only analog part is the comparator, whose design is close to that of a digital regenerative latch. This means that no static current flows if charge leakage from the capacitor digital-to-analog converter (CDAC) can be avoided; hence, the power consumption will be a linear function of the conversion rate.

In fact, a low-power pipelined ADC that does not require amplifiers has been developed. However, the pipeline architecture has more circuits than the SAR architecture. Hence, SAR architecture would still be a better choice for low-power and compact ADCs. Designing the ADC using small devices takes advantage of the scaling merits. Higher conversion rate and smaller area are direct benefits. Smaller area in turn contributes to reducing the power consumption, because the smaller parasitic reduce the required drive power.The SAR ADC samples input signal on the sampling capacitors, Csp and Csn, via the bootstrapped switches, Sa and S_b .The nonlinear variation of the parasitic capacitance during the conversion phase, induced by the sampling switch Sa and the comparator input pair, affects the linearity of the proposed SAR ADC.The top-plate parasitic capacitance of the sampling capacitor is a constant value, which does not affect the ADC performance.

D. DYNAMIC COMPARATOR

The block diagrammatic representation based on the dynamic comparator with preamplifier is given below.

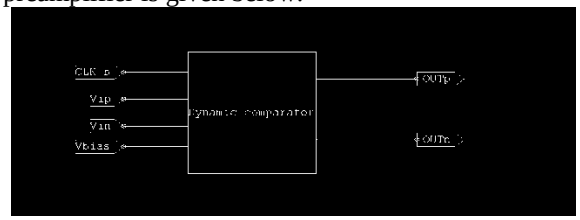

Fig 6 Block diagram of the dynamic comparator

The fig 6 shows the block diagram of a dynamic comparator whose inputs are a clock signal, p channel input voltage, n channel input voltage and bias voltage. When clkc is high, the comparator outputs outp and outn are reset to high. When clkc goes to low, the differential pair compares the two input voltages,The input signals are amplified and produce the output signals.The corresponding layout design of the dynamic comparator based on the block diagram is shown below fig 7

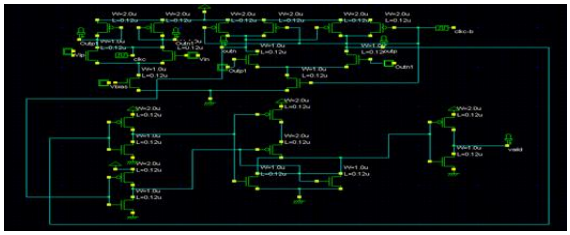

Fig 7 Schematic of the dynamic comparator

The schematic of the comparator is shown above. With a less sampling capacitance the noise generated from the latch comparator becomes more critical. The bottom plate of the sampling capacitors .C_{sp} and C_{sn} are floating and they are more sensitive to noise than the conventional case. Therefore the present comparator approaches a pre-amplifier to block the noise and improve the comparison speed. The Valid signal is pulled to high to enable the asynchronous control clock. The comparator size can be enlarged, which results in larger power consumption. The effective voltage of the input pair can be reduced, but this decreases the comparison speed.

Proposed Dual-TAIL Comparator

The schematic diagram of proposed dual-tail comparator is shown below. Due to the better performance of dual-tail architecture in low-voltage applications, the proposed comparator is designed based on the dual tail structure. The main idea of the proposed comparator is to increase Vfn/fp in order to increase the latch regeneration speed. For this purpose, two control transistors (*M*c1 and *M*c2) have been added to the first stage in parallel to *M*3/*M*4transistors but in a cross-coupled manner.

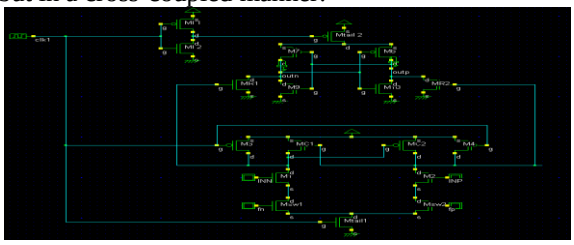

Fig 8. Schematic proposed comparator

The operation of the proposed comparator in the reset phase (CLK = 0, *M*tail1 and *M*tail2 are off, avoiding static power), *M*3 and *M*4 pulls both fn and fp nodes to *V*DD, hence transistor *M*c1 and *M*c2 are cut off. Intermediate stage transistors, *M*R1 and *M*R2, reset both latch outputs to ground. During decision-making phase (CLK = *V*DD, *M*tail1, and *M*tail2 are on), transistors *M*3 and *M*4 turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since fn and fp are about *V*DD). Thus, fn and fp start to drop with different rates according to the input voltages. Suppose *V*INP > *V*INN, thus fn drops

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faster than fp, (since *M*2 provides more current than *M*1). As long as fn continues falling, the corresponding pMOS control transistor (*M*c1 in this case) starts to turn on, pulling fp node back to the *V*DD; so another control transistor (*M*c2) remains off, allowing fn to be discharged completely. In other words, unlike conventional dual-tail dynamic comparator, in which *V*fn/fp is just a function of input transistor transconductance and input voltage difference, in the proposed structure as soon as the comparator detects that for instance node fn discharges faster, a pMOS transistor(*M*c1) turns on, pulling the other node fp back to the *V*DD.Therefore by the time passing, the difference between fn and fp (*V*fn/fp) increases in an exponential manner, leading to the reduction of latch regeneration time . Despite the effectiveness of the proposed idea, one of the points which should be considered is that in this circuit, when one of the control transistors (e.g., *M*c1) turns on,a current from *V*DD is drawn to the ground via input and tail transistor (e.g., *M*c1, *M*1, and *M*tail1), resulting in static power consumption. To overcome this issue, two nMOS switches are used below the input transistors [*M*sw1 and *M*sw2]. At the beginning of the decision making phase, due to the fact that both fn and fp nodes have been pre-charged to *V*DD (during the reset phase), both switches are closed and fn and fp start to drop with different discharging rates. As soon as the comparator detects that one of the fn/fp nodes is discharging faster, control transistors will act in a way to increase their voltage difference. Suppose that fp is pulling up to the *V*DD and fn should be discharged completely, hence the switch in the charging path of fp will be opened (in order to prevent any current drawn from *V*DD) but the other switch connected to fn will be closed to allow the complete discharge of fn node. In other words, the operation of the control transistors with the switches emulates the operation of the latch.

Simulation Result

In order to compare dual tail comparator and dynamic comparator the power consumption and area are reduces due to number of transistor used in the dual tail comparator. The simulation result of dual tail comparator is given below

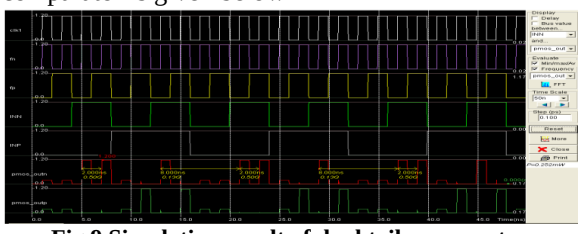

Fig 9.Simulation result of dual tail comparator

Discussion Based On The Simulation Result

The below table represented comparison of dynamic comparator(existing) and dual tail comparator(proposed) performance parameters.

Comparator Structure	Dynamic Comparator	Dual tail Comparator
Architecture	SAR	SAR
Power(mW)	2.2	0.252
Area(μm^2)	0.4	0.1
Delay/log(ps/dec)	940	294
Maximum sampling frequency rate	900MHz	2.4GHz
Energy per conversion(J)	0.3p	0.24p

TABLE 1.Comparison of comparators performance

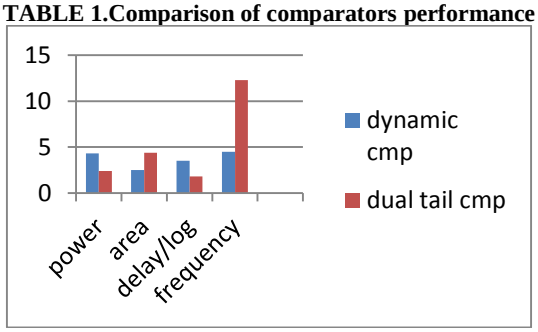

Fig 10.Graphical representation based on the above table

The graphical representation based on the above table details according to the voltage versus time is shown.

Conclusion

In this paper the dual comparator compared with dynamic comparator simulation results the ADC design to optimize power and area, maximize speed and clock frequency. According to an analytical expressions, designers can obtain an intuition about the main contributors to the comparator delay and fully explore the tradeoffs in dynamic comparator is proposed in the circuit of a dual tail comparator. Dual tail comparator is modified for low power and fast operations even in small supply voltages by adding few transistors, positive feedback during the regeneration is strengthened, it results to reduce delay time in the layout simulation results by using CMOS technology analysis.

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